

Ayush Paudel

662-701-8661 | paudela1@msu.edu | linkedin.com/in/Ayush-Paudel

PROFILE:

I am a passionate individual with a deep interest in the latest advancements in silicon technologies, microcontrollers, and VLSI. With a natural curiosity and a drive to constantly improve my skills, I am dedicated to find an opportunity at the forefront of this dynamic field.

EDUCATION:

Master of Science in Electrical and Computer Engineering

Michigan State University, GPA: 3.79/4.00;

Expected Graduation: May 2023

Bachelor of Science in Electrical Engineering

University of Mississippi, May 2021

SKILLS:

- Python: Algorithm design, Pandas, Data visualization
- Verilog: FPGA logic design, Routing, Timing analysis
- C++: Multi-thread programming, OOP, Memory management
- MATLAB: Simulations, Vector operations, Solving ODEs and PDEs

EXPERIENCE:

Nanoelectronics, Plasma and Accelerator Technology Group, Graduate Research Assistant Aug 2021 – Present

- Designed an eigen-model for coupled-cavity travelling wave tubes as an alternative to high computational cost fluid simulations.
- Performed accuracy tests using MATLAB and Python and was able to match the accuracy with the results of particle in cell simulations.
- Collaborated with decorated researchers to analyze and dissect theoretical problems in the broad field of high-power microwaves and plasmas.
- Attended conferences and workshops to present research findings and network with leading figures in the academia as well as industry.

INDIVIDUAL PROJECTS:

- **Hardware Implementation of Advanced Encryption System (AES-128):**

Collaborated with fellow group members to design AES encryption and decryption in Verilog and implement it between two FPGA Boards for secure data transfer. Synthesized the UART module for communication, designed the key generation algorithm, improved the cohesiveness of the design as well as optimized the timing issues with FETs.

- **Blockchain Programming:**

Built a single node blockchain with user defined blocks in Python to demonstrate information flow in a blockchain network.

- **Phono Amplifier PCB Design:**

Designed a phono amplifier using both discrete components as well as Op-Amps to study the frequency response and gain stability of both. PCB designed using Altium Designer.

PUBLICATION:

- Paudel, P. Zhang, P. Wong, J. W. Luginsland and M. A. Franzi, "A Discrete Cavity Analysis for Coupled-Cavity Travelling Wave Tubes," *2022 ICOPS*, Seattle, WA, USA, doi:10.1109/ICOPS45751.2022.9813326

CERTIFICATES:

- Graduate certificate in Computational Modeling
Department of Computational Mathematics, Science & Engineering (CMSE)